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METHOD AND APPARATUS FOR SELECTING AN ENCRYPTION INTEGRATED CIRCUIT OPERATING MODE

RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application No. 10/176,704, filed June 20, 2002, which is now a U.S. Patent 6,664,803 which is a continuation of U.S. Application No. 09/862,339 filed May 23, 2001, now a U.S. Patent 6,466,048. The entire teachings of the above applications are incorporated herein by reference.

Background of the invention

[0002] Integrated circuits are designed typically to operate in two distinct modes, but not at a same time, including a test mode, and a work mode for performing normal processing functions. Integrated circuits of this type are generally referred to as designed for test (DFT). When operating in the test mode, a designer has access to electronic information internal to the integrated circuit, including the contents of memory registers and the step-by-step microcode that is executed within the microprocessor. After a testing operation is completed, the designer switches the integrated circuit to the work mode, and normal processing operations of the integrated circuit are performed.

[0003] Entry into the test mode for integrated circuits is often accomplished through one of dynamic entry and static entry. Dynamic entry into the test mode is accomplished by clocking and latching the required test mode condition into the device